CLAIMS

We claim:

1. An apparatus comprising:

a determine pass logic having inputs coupled to receive significance state information for a region, a pass bit for each coefficient in a subset of the region, and a current pass indication, the determine pass logic to generate pass indications to indicate a pass for each coefficient in the subset of the region;

selection logic having inputs coupled to signals output from the determine pass logic and the current pass indication to generate output indications associated with one pass of either the significance propagation, refinement, and cleanup passes;

next coefficient logic coupled to the selection logic to indicate the next coefficient in the current pass in response to the output indications from selection logic; and

a control coupled to receive the output indicating the next coefficient in the one pass, the control coding coefficients in the significance propagation, refinement and cleanup passes, including coding the next

coefficient in either the significance propagation, refinement and cleanup passes as indicated by the next coefficient logic.

2. The apparatus defined in Claim 1 further comprising next pass bit logic to set a next pass bit indication to indicate state of the next pass bit.

3. The apparatus defined in Claim 2 wherein the next pass bit indicates to control whether to code a 0 or a 1 in the significance propagation pass.

4. The apparatus defined in Claim 2 wherein the next pass bit logic sets the next pass bit indication to not be the same state as the next significance state if in the significance propagation pass when another coefficient in the significance propagation pass had been found.

5. The apparatus defined in Claim 2 wherein the next pass bit logic sets the next pass bit indication to one for all coefficients of the subregion in the refinement pass.

6. The apparatus defined in Claim 2 wherein if the significance state indicates that the coefficient is significance and the current pass bit is in a first state and the pass bit is in the first state, the next significance state indicates the next coefficient to be significance and the next pass bit remains in the same state when in the refinement pass.

7. The apparatus defined in Claim 2 wherein if significance state indicates a coefficient is not significant and the current pass bit is in a first logic state, then the significance state of a next coefficient in the cleanup pass is in the first logic state and the next pass bit is the same as the current pass bit when in the cleanup pass.

8. The apparatus defined in Claim 1 wherein the next coefficient logic comprises:

a mask unit having an input coupled to receive the output indications from selection logic and an identification indicator of a current coefficient in the subset of the region that is being processed, the mask unit outputting a masked version of the output indications; and

a priority encoder coupled to the mask unit and having an output indicating the next coefficient in the current pass, the priority encoder locating each coefficient in the current pass.

9. The apparatus defined in Claim 1 wherein the pass indications comprise significance pass, refinement and cleanup signals.

10. The apparatus defined in Claim 9 wherein each of the significance pass, refinement and cleanup signals includes a plurality of signals, one of the plurality of signals corresponding to each coefficient in the subregion.

11. The apparatus defined in Claim 10 wherein the selection logic comprises a 3:1 multiplexor having inputs coupled to the significance pass, refinement and cleanup signals and having an output to output either the significance pass, refinement or cleanup signals in response to the current pass signal.

12. The apparatus defined in Claim 1 wherein the region comprises a 6x6 region.

13. The apparatus defined in Claim 1 wherein the subregion comprises a 4x4 region.

14. The apparatus defined in Claim 1 wherein the selection logic comprises a 3:1 multiplexor.

15. The apparatus defined in Claim 14 wherein inputs of the multiplexor are 16 bits wide.

16. An apparatus comprising:

a determine pass logic/having inputs coupled to receive significance state information for a region, a pass bit for each coefficient in a subset of the region, and a current pass indication, the determine pass logic to generate pass indications to indicate a pass for each coefficient in the subset of the region;

selection logic having inputs coupled to signals output from the determine pass logic and the current pass indication to generate output indications associated with one pass of either the significance propagation, refinement, and cleanup passes;

a mask unit having an input coupled to receive the output indications from selection logic and an identification indicator of a current coefficient in the subset of the region that is being processed, the mask unit outputting a masked version of the output indications; and

a priority encoder coupled to the mask unit and having an output indicating the next coefficient in the current pass, the priority encoder locating each coefficient in the current pass; and

a control coupled to receive the output indicating the next coefficient in the one pass, the control coding coefficients in the significance propagation, refinement and cleanup passes, including coding the next coefficient in either the significance propagation, refinement and cleanup passes as indicated by the next coefficient logic; and

next pass bit logic to set a next pass bit indication to indicate state of the next pass bit.

17. The apparatus defined in Claim 16 wherein the next pass bit indicates to control whether to code a 0 or a 1 in the significance propagation pass.

18. The apparatus defined in Claim 16 wherein the next pass bit logic sets the next pass bit indication to not be the same state as the next significance state if in the significance propagation pass when another coefficient in the significance propagation pass had been found.

19. The apparatus defined in Claim 16 wherein the next pass bit logic sets the next pass bit indication to one for all coefficients of the subregion in the refinement pass.

20. The apparatus defined in Claim 16 wherein if the significance state indicates that the coefficient is significance and the current pass bit is in a first state and the pass bit is in the first state, the next significance state indicates the next coefficient to be significance and the next pass bit remains in the same state when in the refinement pass.

21. The apparatus defined in Claim 16 wherein if significance state indicates a coefficient is not significant and the current pass bit is in a first logic state, then the significance state of a next coefficient in the cleanup pass is in the first logic state and the next pass bit is the same as the current pass bit. when in the cleanup pass.

22. The apparatus defined in Claim 16 wherein the pass indications comprise significance pass, refinement and cleanup signals.

23. The apparatus defined in Claim 22 wherein each of the significance pass, refinement and cleanup signals includes a plurality of signals, one of the plurality of signals corresponding to each coefficient in the subregion.

24. The apparatus defined in Claim 23 wherein the selection logic comprises a 3:1 multiplexor having inputs coupled to the significance pass, refinement and cleanup signals and having an output to output either the significance pass, refinement or cleanup signals in response to the current pass signal.

25. The apparatus defined in Claim 16 wherein the region comprises a 6x6 region.

26. The apparatus defined in Claim 16 wherein the subregion comprises a 4x4 region.

27. The apparatus defined in Claim 16 wherein the selection logic comprises a 3:1 multiplexor.

28. The apparatus defined in Claim 27 wherein inputs of the multiplexor are 16 bits wide.